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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/561,783	06/19/2006	Brendan P. Kelly	GB03 0080 US	5854

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EXAMINER	
VELEZ, ROBERTO	

ART UNIT	PAPER NUMBER
2829	

NOTIFICATION DATE	DELIVERY MODE
02/19/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/561,783	KELLY, BRENDAN P.	
	Examiner	Art Unit	
	Roberto Velez	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 January 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 01/26/2009 has been entered.

Response to Arguments

2. Applicant's arguments with respect to claims 1-14 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 9-11 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Regarding claim 9, the limitation "the comparison circuit...**for current driving the control input** that is connected to the main and sense cells" was not described in

the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

In page 6, lines 15-18, the specification discloses "A comparator 18 is connected with its positive input connected to the output terminal, its negative input connected to the comparison node and its output connected to a low current output terminal 21 for providing a low current indication". This is not the same to what is being claimed, i.e., "wherein the comparison circuit...**for current driving the control input** that is connected to the main and sense cells". Applicant is welcomed to point out where in the specification the Examiner can find support for this limitation, if Applicant believes otherwise.

Regarding claim 10, the limitation "the comparison circuit...**to drive the control input**" was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

In page 6, lines 15-18, the specification discloses "A comparator 18 is connected with its positive input connected to the output terminal, its negative input connected to the comparison node and its output connected to a low current output terminal 21 for providing a low current indication". This is not the same to what is being claimed, i.e., "the comparison circuit...**to drive the control input**". Applicant is welcomed to point out where in the specification the Examiner can find support for this limitation, if Applicant believes otherwise.

Claim 11 depending from claim 9 is rejected for the same reasons.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-3, 5-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Pulvirenti et al. (US Pat. 5,760,613).

Regarding claim 1, Pilvirenti et al. shows (Fig. 4) a power semiconductor device, comprising: an output transistor [M11, M10] having main cells [M10] and sense cells [M11] (Col. 7, Ln 18-22 and Col. 9, Ln 20-24), a control input [14] connected to the main and sense cells, and main and sense cell controlled outputs [D10, S10, D11, S11]; an output terminal [O5] connected to one of the main cell controlled outputs [S10] for connection to a load [L]; a feedback circuit [13] for measuring (using [I11] the voltage across the main cell controlled outputs [D10, S10] of the output transistor and controlling (using M12) the voltage on the control input to increase the voltage across the main cell controlled outputs if the magnitude of the voltage across the controlled outputs falls below a predetermined value (Col. 9, Ln 54 through Col. 10, Ln 5); a reference current supply [GN7] feeding a reference current through the sense cell controlled outputs; and a comparator [11] arranged to compare the voltages across the main cell controlled outputs and the sense cell outputs and to output a low-current

signal when the magnitude of the voltage across the main cell controlled outputs falls below that across the sense cell outputs (Col. 8, Ln 3-66).

Regarding claim 2, Pilvirenti et al. discloses everything as claimed above in claim 1; in addition, Pilvirenti et al. shows (Fig. 4) wherein the feedback circuit [13] includes a voltage reference [GN8] and a comparator [12] connected across the main cell outputs for comparing the voltage across the main cell outputs with the voltage reference, the output [G12] of the comparator of the feedback circuit being connected through a diode [M12] (note that a transistor consists of two diodes) to the control input [14], the diode being orientated to pass current to change the control voltage in a direction to increase the on-resistance of the main cells when the voltage across the main cell outputs falls below the predetermined value.

Regarding claim 3, Pilvirenti et al. discloses everything as claimed above in claim 1; in addition, Pilvirenti et al. shows (Fig. 4) wherein the main and sense cells are FET main and sense cells [M10, M11] and the gates [G10, G11] of the FETs are connected in common to the control input [14] and the sources [S10, S11] and drains [D10, D11] of the FETs of the main and sense cells form the outputs of the FETs.

Regarding claim 4, Pilvirenti et al. discloses everything as claimed above in claim 3; in addition, Pilvirenti et al. shows (Fig. 4) in the form of a high side device wherein: the drains [D10, D11] of the sense and main cells are connected in common to a battery terminal [V_S]; the source [S10] of the main cells is connected to the output terminal [O5]; and the source [S11] of the sense cells is connected to the reference current supply [GN7], the reference current supply is a reference current sink.

Regarding claim 5, Pilvirenti et al. shows (Fig. 4) a power semiconductor circuit [10] including a power semiconductor device according to claim 1 further comprising a load [L] connected to the output terminal [O5].

Regarding claim 6, Pilvirenti et al. shows (Fig. 4) a method of operating a semiconductor device, the device including an output transistor circuit [M10, M11] having main cells [M10] and sense [M11] cells (Col. 7, Ln 18-22 and Col. 9, Ln 20-24), a control input [14] connected to the main and sense cells, and main and sense cell controlled outputs [D10, S10, D11, S11], the method comprising: driving (using Vs) the main and the sense cells in common; driving (using GN7) a load from one of the main cell controlled outputs feeding a reference current through the sense cell controlled outputs; measuring (using 13) the voltage across the main cell controlled outputs and controlling the voltage on the control input to increase the voltage across the main cell controlled outputs if the magnitude of the voltage across the main cell controlled outputs fails below a predetermined value (Col. 9, Ln 54 through Col. 10, Ln 5); and comparing (using 11) the voltages across the main cell controlled outputs and the sense cell controlled outputs and outputting (using O6) a low-current signal when the magnitude of the voltage across the main cell controlled outputs falls below that across the sense cell controlled outputs (Col. 8, Ln 3-66).

Regarding claim 7, Pilvirenti et al. discloses everything as claimed above in claim 6; in addition, Pilvirenti et al. shows (Fig. 4) wherein the step of measuring the voltage across the main cell controlled outputs is performed by: comparing (using 12) the

voltage across the main cell controlled outputs with a reference voltage (V_R) using a comparators [12]; and driving the control input [14] from the output [G12] of the comparator through a diode [M12] the diode being orientated to pass current to change the control input voltage in a direction to increase the on-resistance of the main cells when the voltage across the main cell outputs falls below the predetermined value.

Regarding claim 8, Pilvirenti et al. shows (Fig. 4) a device comprising: an output transistor circuit [M10, M11] having main cells [M10] and sense [M11] cells (Col. 7, Ln 18-22 and Col. 9, Ln 20-24); a control input [14] connected to the main and sense cells; main and sense cell controlled outputs [D10, S10, D11, S11]; a first circuit [V_S] configured and arranged to drive the main and the sense cells in common; a second circuit [GN7] configured and arranged to drive a load from one of the main cell controlled outputs feeding a reference current through the sense cell controlled outputs; a measurement circuit [13] configured and arranged to measure the voltage across the main cell controlled outputs and controlling the voltage on the control input to increase the voltage across the main cell controlled outputs if the magnitude of the voltage across the main cell controlled outputs falls below a predetermined value (Col. 9, Ln 54 through Col. 10, Ln 5); and a comparison circuit [11] configured and arranged to compare the voltages across the main cell controlled outputs and the sense cell controlled outputs and outputting a low-current signal when the magnitude of the voltage across the main cell controlled outputs falls below that across the sense cell controlled outputs (Col. 8, Ln 3-66).

Regarding claim 9, Pilvirenti et al. discloses everything as claimed above in claim 8; in addition, Pilvirenti et al. shows (Fig. 4) wherein the comparison circuit [11] is further configured and arranged to output the low-current signal for current driving the control input that is connected to the main and sense cells (Col. 8, Ln 3-66).

Regarding claim 10, Pilvirenti et al. discloses everything as claimed above in claim 9; in addition, Pilvirenti et al. shows (Fig. 4) wherein each of the main and sense cells [M10, M11] includes a FET-based circuit with a gate terminal [G10, G11], and the comparison circuit [11] is further configured and arranged to drive the control input [14] by outputting the low-current signal [O6].

Regarding claim 11, Pilvirenti et al. discloses everything as claimed above in claim 9; in addition, Pilvirenti et al. shows (Fig. 4) wherein each of the main and sense cells [M10, M11] includes a FET-based circuit with a gate terminal [G10, G11], and wherein the control input [14] is commonly connected to each gate terminal of the main and sense cells for driving the main and sense cells.

Regarding claim 12, Pilvirenti et al. discloses everything as claimed above in claim 8; in addition, Pilvirenti et al. shows (Fig. 4) further including a load [L] connected between an output terminal [O5] of the output transistor and ground [GND].

Regarding claim 13, Pilvirenti et al. discloses everything as claimed above in claim 8; in addition, Pilvirenti et al. shows (Fig. 4) further including a battery [GN8] arranged for providing a voltage reference [V_R] to the measurement circuit [13], and providing power to the main and sense cells [M10, M11].

Regarding claim 14, Pilvirenti et al. discloses everything as claimed above in claim 8; in addition, Pilvirenti et al. shows (Fig. 4) further including a battery [GN8] arranged for providing a voltage reference [V_R] to the measurement circuit [13] and for providing power to the main and sense cells, and further including load [L] connected between an output terminal [O5] of the output transistor and ground [GND].

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Tihanyi et al. (US Pat. 5,815,027) discloses a circuit configuration for detecting a load current of a power semiconductor component with a source-side load.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Roberto Velez whose telephone number is 571-272-8597. The examiner can normally be reached on Monday-Friday 8:00am- 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on 571-272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Roberto Velez/
Examiner, Art Unit 2829
02/13/2009

/Ha T. Nguyen/
Supervisory Patent Examiner, Art Unit 2829